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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ECKERT II, GEORGE C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/688,692	RIM, KERN	
	Examiner	Art Unit	
	George C. Eckert II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *10-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 10-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on January 28, 2005.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claim 1, on lines 5-6, the claim states that the "source/drain *junction,*" which is formed in a second semiconductor layer, extends to a first buried insulator but that the buried layer is isolated from the second semiconductor layer by a first semiconductor layer and a second buried insulator. As the term is used in the art, a *junction* is a meeting point of two differently doped regions. As such, it is not clear how the source/drain *junction* can extend to a first buried layer but have a second semiconductor layer intervening. For this action, the limitation will be treated such that the source/drain *region* extends to the first buried insulator.

Also regarding claim 1, on lines 9-10, the limitation "a first semiconductor layer" is cited. However, this limitation was previously cited so that it is not clear if the same layer is being referenced or if it is a different layer. Regarding claims 2 and 3, both claims cite "an isolation region" and "a device" but it is not clear if it is the same isolation region or device as cited in claim 1 or a new one. The remaining claims are rejected based on their dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 3-7 are rejected under 35 U.S.C. 102(b) as being anticipated by 6,424,020 to Vu et al. With regard to claim 1 as best understood, Vu teaches in figure 17D, an SOI MOSFET comprising:

an elevated device region having at least one semiconductor device (a MOSFET) located on a second semiconductor layer 1214, wherein said elevated device region further comprises a source/drain junction (the n+ region on the far left of layer 1214) which extends from the second semiconductor layer 1214 down to a first buried insulator layer (1204) (the extension by means of the conductor 1228) that is located on an upper surface of a semiconductor substrate 1206, the first buried insulator is separated from the second semiconductor layer 1214 by a first semiconductor layer 1202 and a second buried insulator layer 1216;

a recessed device region having at least one semiconductor device (a MOSFET) located atop a first semiconductor layer 1202 which is located on an upper surface of the first buried insulator 1204; and

an isolation region 1226 separating the elevated device region from the recessed device region.

Regarding claim 3 as best understood, Vu teaches that the source/drain junction formed in the elevated region is not self-aligned to an isolation region or a spacer (note the process of

fig. 17A showing that the source/drain junction is formed prior to the neighboring isolation 1210 and that there are no spacers in the final device of fig. 17D). Regarding claims 4-7, Vu teaches that the first and second semiconductor layers comprise the same material (Si), are not strained (since they are not taught to be strained), are homogeneous and have either the same or different crystal orientation (Vu teaches that both layers are single crystal and it is inherent that they are either the same or differently oriented, col. 16, lines 28-40).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 2 as best understood is rejected under 35 U.S.C. 103(a) as being unpatentable over 6,424,020 to Vu in view of 5,482,871 to Pollack. As the claim is best understood, Vu teaches the device of claim 1. However, Vu did not teach that the source/drain junction region is self-aligned to an edge of an isolation region and a spacer of a device located within the elevated device region. Pollack teaches in figure 8 an SOI device wherein the source/drain junction region 48 of the device 100 is self-aligned to the spacer 45 and aligned to an edge of an isolation region 50.

Vu and Pollack are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the device of Vu having the source/drain junction aligned to a spacer and isolation region. The

motivation for doing so, as is taught by Pollack, is that the spacers 45 allow a dual implant to form LDD regions first (which reduce short channel effects) and then the source/drain junction region (col. 6, lines 44-55) and the use of an isolation region or spacer on the side of the silicon layer (e.g. 38 or 50) allows formation of the gate electrode while avoiding stringers that would otherwise defeat proper operation of a mesa-isolated SOI transistor (col. 6, lines 21-28). Therefore, it would have been obvious to combine Vu and Pollack to obtain the invention of claim 2.

5. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,424,020 to Vu et al. in view of 4,933,298 to Hasegawa. As the claim is best understood, Vu teaches the device of claim 1 as discussed. However, Vu did not teach that the devices formed therein were a pFET with a (110) orientation and an nFET with a (100) orientation. Hasegawa teaches in figure 3h, the formation of two SOI devices in different areas, the area 3AR having a (110) orientation and a pFET formed therein and the area 3BR having a (100) orientation and an nFET formed therein (see col. 4, lines 6-42).

Vu and Hasegawa are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the device of Vu wherein a pFET is formed in a layer having a (110) orientation and an nFET is formed in an area having a (100). The motivation for doing so, as is taught by Hasegawa, is that such formation exploits the greater mobility of the carriers in both types of devices respectively (col. 5, lines 20-29). Therefore, it would have been obvious to combine Vu and Hasegawa to obtain the invention of claims 8 and 9.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additional cited art teaches various elevated SOI structures.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (571) 272-1728.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GEORGE ECKERT
PRIMARY EXAMINER